| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| NEG | Reg | 3 | 2 |
| | Mem | 16 + EA | 2-4 |
| DEC, INC | 16-bit Reg | 2 | 1 |
| | 8-bit Reg | 3 | 2 |
| | Mem | 15 + EA | 2-4 |
| ADD, SUB | Reg → Reg | 3 | 2 |
| | Mem → Reg | 9 + EA | 2-4 |
| | Reg → Mem | 16 + EA | 2-4 |
| | Immediate → Reg | 4 | 3-4 |
| | Immediate → Mem | 17 + EA | 3-6 |
| | Immediate → Acc | 4 | 2-3 |
| CMP | Reg → Reg | 3 | 2 |
| | Mem → Reg | 9 + EA | 2-4 |
| | Reg → Mem | 9 + EA | 2-4 |
| | Immediate → Reg | 4 | 3-4 |
| | Immediate → Mem | 10 + EA | 3-6 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| CBW | Convert byte to word | 2 | 1 |
| CWD | Convert word to double word | 5 | 1 |
| MUL | 8-bit Reg | 70 – 77 | 2 |
| | 16-bit Reg | 118 – 133 | 2 |
| | 8-bit Mem | (76 – 83) + EA | 2-4 |
| | 16-bit Mem | (124 – 139) + EA | 2-4 |
| IMUL | 8-bit Reg | 80-98 | 2 |
| | 16-bit Reg | 128 – 154 | 2 |
| | 8-bit Mem | (86 – 104) + EA | 2-4 |
| | 16-bit Mem | (134 – 160) + EA | 2-4 |
| DIV | 8-bit Reg | 80 - 90 | 2 |
| | 16-bit Reg | 144 - 162 | 2 |
| | 8-bit Mem | (86 – 96) + EA | 2-4 |
| | 16-bit Mem | (150 – 168) + EA | 2-4 |
| IDIV | 8-bit Reg | 101 – 112 | 2 |
| | 16-bit Reg | 165 – 184 | 2 |
| | 8-bit Mem | (107 – 118) + EA | 2-4 |
| | 16-bit Mem | (171 – 190) + EA | 2-4 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| NOT | Reg | 3 | 2 |
| | Mem | 16 + EA | 2-4 |
| AND, OR, XOR | Reg → Reg | 3 | 2 |
| | Mem → Reg | 9 + EA | 2-4 |
| | Reg → Mem | 16 + EA | 2-4 |
| | Immediate → Reg | 4 | 3-4 |
| | Immediate → Mem | 17 + EA | 3-6 |
| | Immediate → Acc | 4 | 2-3 |
| RCL, RCR, ROL, ROR, SAL/SHL, SAR/SHR | Reg with 1 shift | 2 | 2 |
| | Reg with variable shift | 8 + 4/bit | 2 |
| | Mem with 1 shift | 15 + EA | 2-4 |
| | Mem with variable shift | 20 = EA + 4/BIT | 2-4 |
| TEST | Reg → Reg | 3 | 2 |
| | Mem → Reg | 9 + EA | 2-4 |
| | Immediate → Acc | 4 | 2-3 |
| | Immediate → Reg | 5 | 3-4 |
| | Immediate → Mem | 11 + EA | 3-6 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| CALL | Intrasegment direct | 19 | 3 |
| | Intrasegment indirect through register | 16 | 2 |
| | Intrasegment indirect through memory | 21 + EA | 2-4 |
| | Intersegment direct | 28 | 5 |
| | Intersegment indirect | 37 + EA | 2-4 |
| RET | Intrasegment | 8 | 1 |
| | Intrasegment with constant | 12 | 3 |
| | Intersegment | 18 | 1 |
| | Intersegment with constant | 17 | 3 |
| Conditional Jump | branch taken | 16 | 2 |
| | branch not taken | 4 | 2 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| JMP | Intrasegment direct short | 15 | 2 |
| | Intrasegment direct | 15 | 3 |
| | Intrasegment direct | 15 | 5 |
| | Intrasegment indirect through memory | 18 + EA | 2-4 |
| | Intrasegment indirect through register | 11 | 2 |
| | Intrasegment indirect | 24 + EA | 2-4 |
| INT | Type 3 | 52 | 1 |
| | Not Type 3 | 51 | 2 |
| LEA | Load effective address | 2 + EA | 2-4 |
| LOOP | branch taken | 17 | 2 |
| | branch not taken | 5 | 2 |
| LOOPE, LOOPZ | branch taken | 18 | 2 |
| | branch not taken | 6 | 2 |
| LOOPNE, LOOPNZ | branch taken | 19 | 2 |
| | branch not taken | 5 | 2 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| MOV | Acc → Mem | 10 | 3 |
| | Mem → Acc | 10 | 3 |
| | Reg → Reg | 2 | 2 |
| | Mem → Reg | 8 + EA | 2-4 |
| | Reg → Mem | 9 + EA | 2-4 |
| | Immediate → Reg | 4 | 2-3 |
| | Immediate → Mem | 10 + EA | 3-6 |
| | Reg → SS, DS, ES | 2 | 2 |
| | Mem → SS, DS, ES | 8 + EA | 2-4 |
| | Seg Reg → Reg | 2 | 2 |
| | Seg Reg → Mem | 9 + EA | 2-4 |
| XCHG | Reg ←→ Acc | 3 | 1 |
| | Reg ←→ Mem | 17 + EA | 2-4 |
| | Reg ←→ Reg | 4 | 2 |
| XLAT | | 11 | 1 |

| Instruction | Description | Clock Cycles | Number of Bytes |
|---|---|---|---|
| POP | Reg | 8 | 1 |
| | Seg Reg SS, DS, ES | 8 | 1 |
| | Mem | 17 + EA | 2-4 |
| PUSH | Reg | 11 | 1 |
| | Seg Reg | 10 | 1 |
| | Mem | 16 + EA | 2-4 |
| POPF | | 8 | 1 |
| PUSHF | | 10 | 1 |

| **EA** | **Number of Clock Cycles** |
|---|---|
| Direct | 6 |
| Register indirect | 5 |
| Register relative | 9 |
| Based indexed | |
| (BP)+(DI) or (BX)+(SI) | 7 |
| (BP)+(SI) or (BX)+(DI) | 8 |
| Based indexed relative | |
| (BP)+(DI)+DISP or (BX)+(SI)+DISP | 11 |
| (BP)+(SI)+DISP or (BX)+(DI)+DISP | 12 |

Yu-cheng Liu and Glenn A. Gibson, *Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design,* Second Edition, Appendix A, Prentice-Hall (1986)